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| **Photo**  **D:\KPP\BPUT FACULTY rEGISTRATON\bput registration data foe ECE Dept\ECE FACULTY\2021-22\PITAMBAR SIR\PHOTO.jpeg** | |  | | --- | | **Name: K. PITAMBAR PATRA**  Designation: Asst. Prof.  **Email: kpitambarpatra@gmail.com**  **Area of Specialization: ECE(VLSI)**  **Affiliation:** Department of Electronics and Communication Engineering, Einstein Academy of Technology & Management, Khordha, Bhubaneswar, Odisha | |

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| **Personal Details:** |
| Date of birth: 15/06/1989  Marital status: Married  Permanent address: AT/PO-PANCHABHUTI, DIST-GANJAM, ODISHA-761121  E-mail: **kpitambarpatra@gmail.com**  Contact Nos.: 9938996989, 7008196591  Skype ID:  Scopus ID:  ISTE Membership No: 135257   |  |  |  | | --- | --- | --- | | **Education:** | | | | ***Degree*** | ***Specialization*** | ***University / Institute*** | | Ph.D |  |  | | ME / M.Tech | ECE(VLSI) | JUET,GUNA | | BE / B.Tech | ETC | BPUT, ROURKELA | |

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| **Academic Experience:** |
| * **Presently working as Asst. Prof at Einstein Academy of Technology & Management , Bhubaneswar From Sept.-2015**  |  |  | | --- | --- | | * **Worked as asst. prof. in RKDF Institute of Science and Technology, Bhopal from July-2014 to Aug-2015.**   **Research Experience: Nil** | | |  | | | **Industrial Experience: Nil** | | |  | | | **Subjects Handled:** | | | **U.G.** |  | | * Signals and systems * Digital Logic Design * Digital Image Processing * Digital System Design * Biomedical Instrumentation * Analog and Digital Communication |  | | **Research Interests: VLSI, Digital Circuits Design, Digital Signal Processing, Communication Engineering** | | |  | | | **Patents Filed / Awarded:** | | |  | | | **Funded Projects:** | | | **Title**  **Funding Agency:**  **Year:** | |  |  | | --- | | **International Journals:** | | |  | | --- | | * **K.Pitambar Patra, Sujit Kumar Patel,: “Area and Power Efficient Modulo Multiplier,”: *International Journal of Modern Engineering Research* ,** Vol.3, Issue.3, May-June 2013 pp-1372-1376**.** * **K. Pitambar Patra, Saket Shrivastava,:** **“An FPGA Based Implementation for 2-D Discrete Wavelet transform,”: *IOSR Journal of Engineering,*** Vol. 3, Issue 5 (May. 2013), ||V4 || PP 21-25. * **K.Pitambar Patra ,Kamna nayak,: “ Study of high speed 32-bit data processing using CSLA,”:Association for *International Journal in computer Science & Electronics*,** Volume. 4,Issue. 3. * **Mansi Gangele, K.Pitambar Patra**,**: “Comparative Analysis Of Lector And Stack Technique To Reduce The Leakage Current In Cmos Circuits,”: *International Journal of Research in Engineering and Technology*  *,*** Volume: 04 Issue: 07 | July-2015. * **K. Pitambar Patra, Swapna Subudhiray,: “Review Paper on VLSI Architecture for Carry Select Adder,”: *International journal of advanced research in computer and communication engineering,*** Volume 5, Issue 1, January 2016. * **K. Pitambar Patra, Swapna Subudhiray,: “High Speed Area Efficient FFT using Modified SQRT CSLA and 5:3 & 9:4 Compressor,”: *International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering,*** Volume 4, Issue 1, January 2016. * **Chinmayee Panda, K. Pitambar Patra, Asutosh Padhy and Urmila Bhanja,:” PDF Analysis of Different Channel Models in FSO,” : Springer Nature Singapore Pte Ltd.** 2020. * **Chinmayee Panda, Sambit Patnaik, K. Pitambar Patra, Asutosh Padhy, Ashisha Kumar Mohanty and Sumit Kumar Choudhary,: “QPSK Modulated Li Fi in Wireless Medium,”** : International Journal of Engineering Research & Technology (IJERT), 2020. * **Chinmayee Panda, K. Pitambar Patra, Asutosh Padhy and Urmila Bhanja,:” PDF Analysis of Different Channel Models in FSO,”:** In book: Advances in Data Science and Management (pp.355-361). | | **Conferences / STTPs / FDPs / Seminars Organized:**   1. FDP ON Machine Learning and Artificial Intelligence Techniques for Communication” in 2020. 2. STTP ON State Of Art in Communication Engineering And Signal Processing, 2021 |   **STTPs / FDPs / Seminars / Workshops Participated:**   * Attended FDP on the topic “RECENT VISTAS ON DEVELOPMENTS IN COMMUNICATION NETWORK” at Regional Telecom Training Center ,BBSR on 21/11/2015. * Attended FDP on the topic “HOW TO PUBLISH PUBLISHABLE MANUSCRIPT” at EATM,BBSR on 20/05/2016. * Attended workshop on “ CMOS, Mixed signal & Radio frequency VLSI design” MHRD, Govt. of India at GIFT, BBSR between 30TH JAN 2017 to 4TH FEB 2017. * Attended International Webinar on” MACHINE LEARNING IN CYBERPSYCHOLOGY STUDIES, at GIET, Baniatangi on 29th May 2020. * Attended International Webinar on “ FUTURE ENERGY CHALLENGES IN GREEN TECHNOLOGY” organized by GIET, Baniatangi ON 9th June 2020. * Attended National Webinar on “ Project completion ideas for students during lockdown” organized by LNCT, Bhopal on 10th June 2020. * Attended National Webinar on “ Foundations to frontiers in 5G Technology” organized by IMPS, MALDA on 26th June 2020. * Attended National Webinar on “ VLSI ARCHITECTURE FOR IMAGE PROCESSING APPLICATIONS” organized by SVPEC, Visakhapatnam on 24th July 2020. * Attended National Webinar on “ Communication & Signal Processing” organized by REC, Bhubaneswar on 10th Oct 2020.   **Achievements and Awards:**   * Received Best Faculty Award in 2019 at EATM, Bhubaneswar. * Branch topper in B-Tech. * School topper in Class 10th Board Exam.   **Professional Society Memberships:** | | |